

10/040852

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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10040852 40040304	FILING DATE 12/27/01 01/09/2002	CLASS 430 116	SUBCLASS 018	GAU 2822 2825	EXAMINER DO
**APPLICANTS: Kasai Naoki;					
**CONTINUING DATA VERIFIED: THIS APPLICATION IS A DIV OF 09/703,807 11/02/2000 PAT 6,340,408					
** FOREIGN APPLICATIONS VERIFIED: JAPAN 11-314462 11/04/1999					
PG-PUB DO NOT PUBLISH <input type="checkbox"/>		RESCIND <input type="checkbox"/>			
Foreign priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO			
35 USC 119 conditions met <input type="checkbox"/> yes <input type="checkbox"/> no		8013-1009-1			
Verified and Acknowledged Examiners's initials					
TITLE : Semiconductor device with reduced number of intermediate interconnection pattern and method of forming the same					
U.S. DEPT. OF COMM./PAT. & TM.-PTO-436L (Rev. 12-94)					

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner		DRAWING	
		Sheets Drwg.	Figs. Drwg.
Primary Examiner		Print Fig.	
PREPARED FOR ISSUE		Application Examiner	
<input type="checkbox"/> TERMINAL DISCLAIMER		WARNING: The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368, Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.	

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